State-Of-The-Art Approach to Mitigate Risk of Die Crack with Substrate Co-Planarity Issue

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***Abstract*— Miniaturization and compact IC package are the main driver for Die Attach Film (DAF) implementation. DAF as alternative to liquid epoxy to overcome problems such as epoxy bleed, uneven bond line thickness (BLT). However, one of the challenges in DAF processing is presence of delamination/ void. This work outlines the correlation between substrate topography with DAF void and die crack. The die crack with fixed location and pattern is caused by void between Die Attach Film (DAF) and substrate. DAF-Substrate separation occurs at the lower side of uneven flatness of DAP which is a "Pivot effect" underneath the die when high packing pressure in mold process and shrinkage during cross linking of mold compound. This eventually leads to die crack. Voids formation can be reduced by optimizing die attach parameter. Based on the DOE conducted, high bond delay and high bond temperature significantly improved on the voids and die crack. These findings provide insights into improving the reliability of IC packaging and optimizing the DAF process for future applications.**

Keywords—DAF, void, die crack, pivot effect

I. INTRODUCTION

With the development of miniaturization of packages, die thickness reduction and compact IC packages have led to denser devices and a wider field of application possibilities. The advancement of electronic devices needs to exhibit more functions, restrain extreme condition and temperature without sustaining any damages to the components. Such advancement of technology also brings new challenges to semiconductor packaging processes. One of the critical processes is the die attach which also known as die bonding or die mount. It is a process of securing a silicon chip to the die attach pad of the semiconductor package's support structure such as substrate or lead frame. There are typically five known methods of attaching die, which is eutectic bonding, soft solder die attach, flip chip die attach, epoxy die attach and tape die attach. Most industry adopt the epoxy die attach method as it is considered to be low-cost and low-powered applications. In this method, the die is directly attached onto the substrate or lead frame using epoxy adhesive. However, this method poses quality risk when epoxy bleed occurs. The epoxy bleed creates a thin layer of contamination at the bond pad area which consequently causing wire non-sticking during the wire bonding process and even have risk of causing wire short. In additional, this method also has high risk of epoxy inconsistency (insufficient or overflow), epoxy on die or lead, and even lifted die due to uneven bond line thickness (BLT). Thus, an alternative method was introduced which is to apply adhesive directly onto the back of the wafer. This method is known as tape die attach, where the tape is often referred to as die attach film (DAF). It is a polymer adhesive which used for non-conductive adhesive applications to achieve good BLT and placement accuracy. Using the wafer backside lamination (WBL) technique, the usage of DAFs in die attach provide industry with plenty of advantages such as process simplification by eliminating the epoxy dispensing process, cost reduction, and reducing thinned wafer breakage. The typical assembly flow of semiconductor packaging with DAF is shown in Fig. 1.

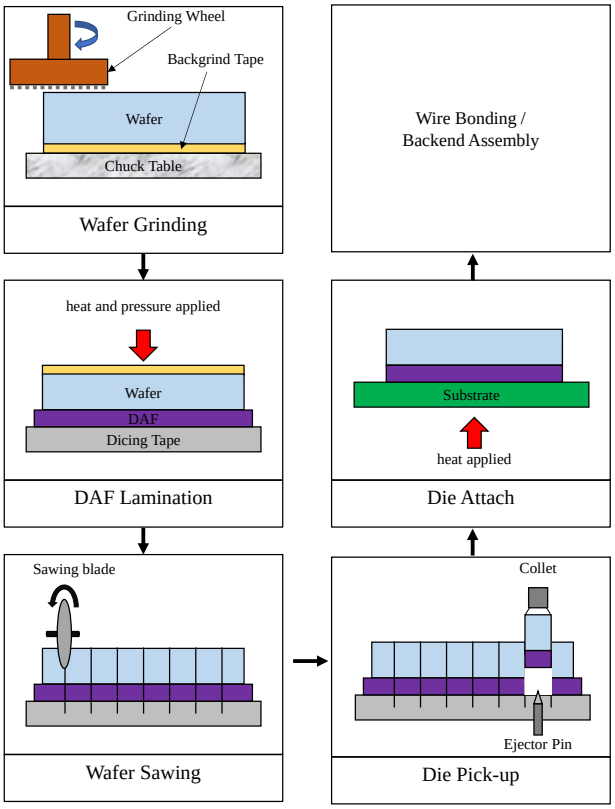


Fig. 1 Assembly process flow with DAF.

However, processing DAF material presents certain difficulties, DAF void is one of the major concerns, which will make the package more susceptible to delamination and cracking. Voids increase moisture absorption, the moisture absorbed in package turn into vapor during reflow process. The stress concentration near voids is responsible for crack initiation. Besides, the void formation at interface degrades adhesive strength [1]. Bin Zhang et al reported that if the voids in die attach are big enough, delamination tend to occur at die to die or die to substrate. This is because the die will not get support in the delamination are against stress from die topside, which greatly increases the possibility of die crack [2]. Study conducted by Yeqing Su et al reported that DAF void can be reduced significantly by enhancement of transfer pressure during molding process, which can be explained that gap on substrate surface is filled furthest by film under high transfer pressure [3].

Besides, substrate plays a crucial role in the occurrence of die crack in IC packages. The substrate is responsible for providing mechanical support to the die and for dissipating the heat generated during device operation. The substrate's design layout can induce various stress distributions that directly affect the IC chip during assembly processes,

leading to die crack damage. Proper substrate layout design is necessary not only to meet the thermal and electrical functional requirements but also to prevent critical mechanical problems. A study conducted by N. Kao et al showed that thicker substrate can reduce more stress serving as an effective solution to die crack damage [4].

The primary objective of this research is to investigate the causes and impact of DAF void in BGA packages. In addition, this study aims to identify ways to improve die attach parameters to reduce void formation.

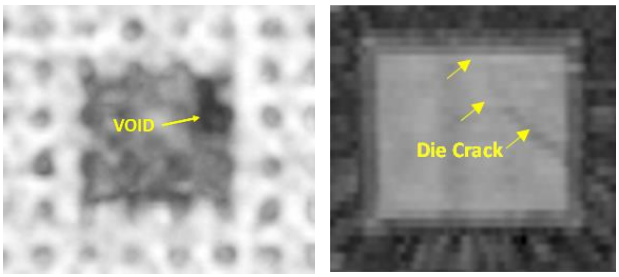
II. EXPERIMENTAL PROCEDURE

A. Material

In this study, a BGA package with size of 14x14mm was employed, and the DAF thickness was measured to be between 22-28um. The die size dimension is 106 x 95mil, with a thickness of 4mil.

B. Methodology

To inspect voids and die cracks, non-destructive analysis was conducted using SAT (Scanning Acoustic Tomography) on encapsulated units. The scanning machine has a 50MHz transducer which enable high resolution images of size as small as 1 micron to be captured. The equipment used is capable to perform two types of modes, which is the transmission (through scan) and reflection (C-Scan). In this study, the presence of void or die crack will be showed in different intensity of the transmitted or reflected wave, where the darker shades indicate the defect location. The transmission mode is an ideal method for detecting voids or delamination located beneath the surface of a material, as the waves penetrate through the material and the resulting intensity differences can be analyzed to create an image of the void. While in the case of reflection mode, it is preferred to use for die crack detection due to its high-resolution image of the internal structure. The different types of mode are shown in Fig. 2



(a) (b)

Fig. 2. SAT image on encapsulated unit (a) transmission mode (through scan) and (b) reflection mode (C-Scan)

For destructive analysis, decapsulation was carried out by mixing Nitric Acid Fuming and Sulphuric Acid 96% using an auto-decapper machine. Cross-section and backside polishing techniques were employed to identify the die crack pattern. Unit was cold molded using epoxy resin and harderner, followed by manual grinding to the die crack region. Backside polishing was carried out by removing solder ball and substrate to reveal the DAF coverage on the unit. Additionally, substrate co-planarity was investigated to study the correlation with DAF void. Furthermore, die attach machine parameters such as bond temperature and bond delay were evaluated to understand their effects on die cracks.

III. RESULT AND DISCUSSION

A. Die Crack Characteristic

The die crack signature can be confirmed through decapsulation of the defective unit by removing the mold compound. The defect signature of this study was observed to be localized at the top right corner with a U-shaped pattern from top edge to right edge as shown in Fig. 3. To further understand die crack characteristic and mechanism, cross-section of the defect unit was performed. Based on the cross-sectional result shows in Fig. 4, the crack was initiated from die top surface and propagated to the bottom of the die. Additionally, no package crack line propagating into die bond region based on the external unit inspection result. This indicated that the die crack was not originated from any external factor or force which would cause the package to crack and propagated to the die. Further analysis observed that DAF void formation was found at the DAF area where the crack propagated. Moreover, DAF void was detected on uneven solder mask area, wherein the area without voids exhibited substrate thickness of 184um, while the substrate thickness at the void area was found to be the lowest, measured 162um as shown in Fig. 5. Further fractography analysis on the defective unit is shown in Fig. 6. It revealed that severe stress initiated from the edge of the die and propagated to the middle of the die,

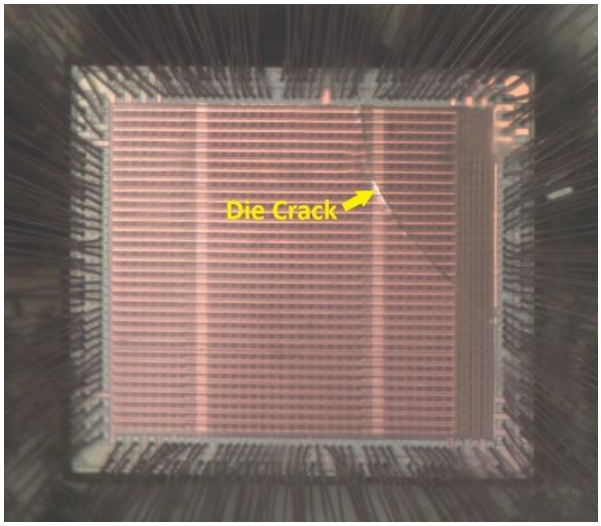
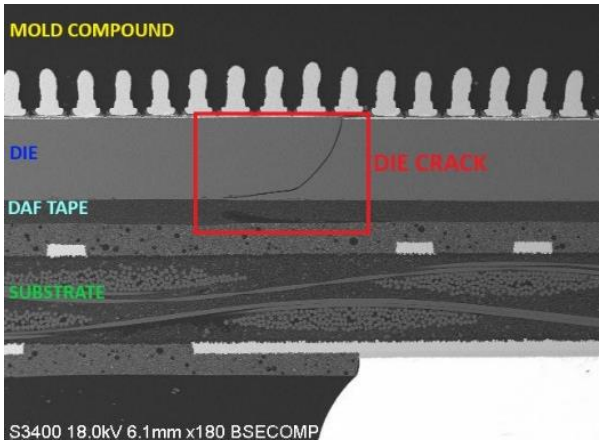
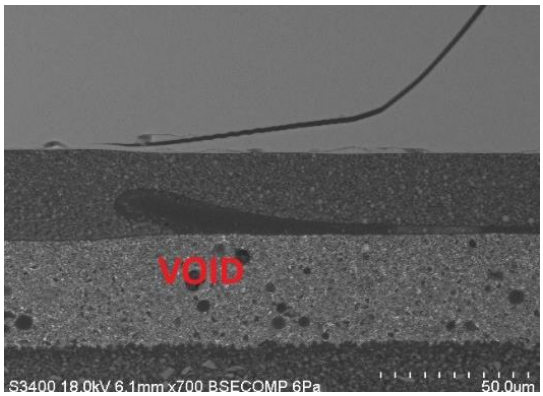


Fig. 3. Optical image on die crack unit after decapsulation.

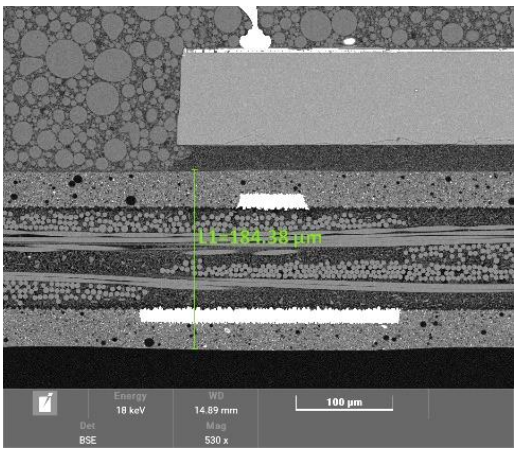


(a)

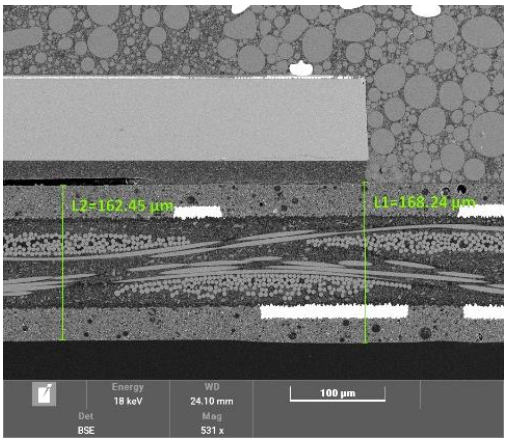


(b)

Fig. 4.Cross-section image of die crack unit at (a) 180x magnification and (b) 700x magnification



(a)



(b)

Fig. 5. Substrate thickness measurement (a) area without void and (b) area with void

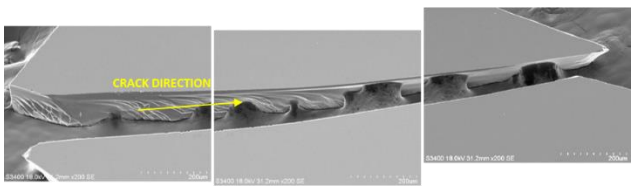


Fig. 6. Fractography Analysis

B. Correlation between substrate and void

Based on the cross-sectional results as aforementioned in Fig 3, it can be observed that the existence of voids was found at the substrate-DAF interface and the location of the void coincides with the area of die crack. Cross-sectional results of the die crack unit also revealed that the area without the crack line, voids cannot be found. This observation indicates that the DAF voids might be the contributing factor that resulted in die crack. Thus, to further understand the correlation between substrate and the formation of void, a 3D measuring laser microscope was employed to investigate the surface topology of a substrate.

Fig.7 shows the result of blank substrate surface topology with die and rubber collet imprinted for better visual understanding. The collet is a device that holds the die during the die attach process. It acts as a vacuum cup that grips the die and accurately positions it onto the substrate or lead frame. From the imprint, it shows that the crack location is not due to the overload force from the bonding process as the crack would have initiated surrounding the collet location. In addition, if hairline crack was detected before molding process, mold compound will sip into the crack. However, in this case, the crack was only detected after mold process and no mold compound was found in the crack. Therefore, the primary contributor to the die crack is suspected to be the substrate surface planarity which lead to the formation of DAF voids. Based on the blank substrate profile shown in Fig.7, observed uneven die attach pad (DAP) surface. Analysis of the surface topology revealed that the die crack area exhibited the lowest height. The red color indicates the highest area, the green color represents the middle position while the blue region represents the lowest area of the surface. The DAF voids formation are believed to form at the region with the lowest height after die attach process.

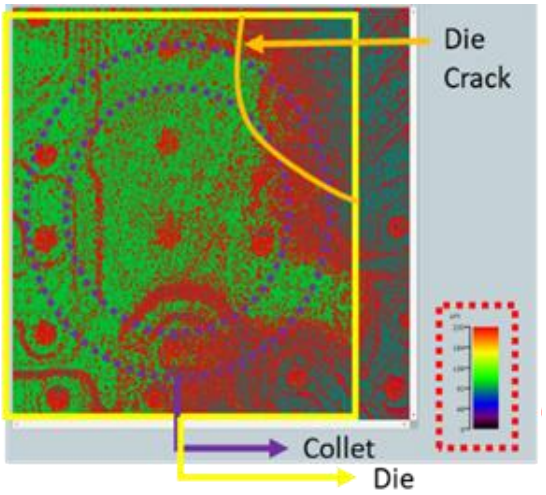


Fig.7. Surface topology of blank substrate with die and collet imprint.

To investigate the DAF void location on the substrate surface, a die crack unit was submitted to failure analysis for backside polishing. This procedure involves removing the solder ball and substrate to reveal the DAF coverage on the unit. Based on the result shown in Fig.8, the DAF tape void location correlated with the region that is significantly lower in depth as aforementioned in Fig.7. The DAF voids region observed also known as DAF-substrate separation would

then act as a "pivot" underneath the die during the high packing pressure in the mold process. The "pivot" effect will cause uneven pressure distribution that eventually leads to higher pressure concentrated at the DAF voids region. The build up pressure would result in fracture or cracking of the die. Fig.9 illustrate the critical mechanism of die crack from the die attach process until the molding process.

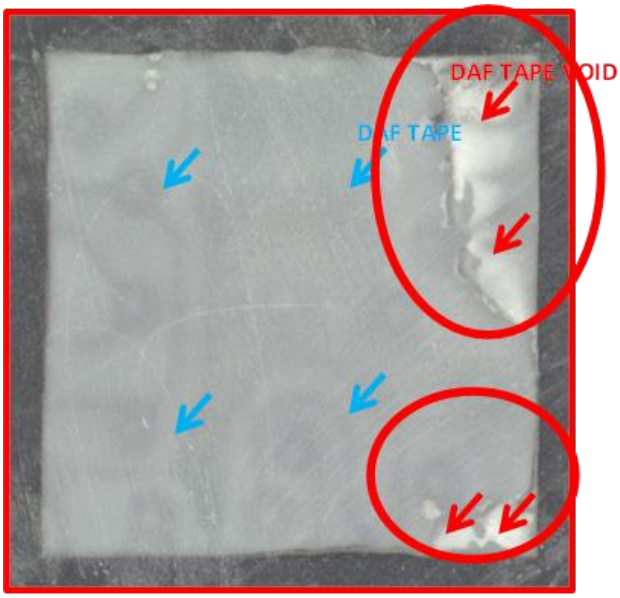


Fig.8. Backside polishing of unit to show the DAF remains.

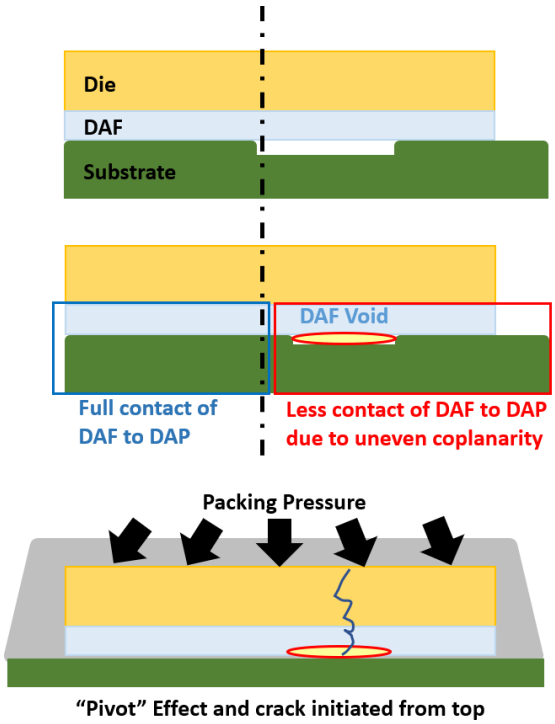


Fig.9. Illustration of die crack mechanism with pivot effect.

C. Die Attach Parameter

The key parameters in die attach process in regards to the DAF void reduction are identified as the bonding temperature and bonding delay. The bonding temperature are regulated with the use of heated block which is also known as an anvil block. It provides a controlled temperature environment for the die bonding process, and also acts as a support block to hold the substrate firmly through vacuum hole opening, it is to ensure the die is bonded accurately onto the specific location of the substrate. The heating element is required when DAF tape is used instead of epoxy as the heat would aid in melting the DAF to ensure partial gripping of the die to prevent the die from shifting away from its bonded location. Additionally, the bonding temperature plays a crucial role in DAF void reduction is because heat is needed to melt the DAF onto the surface of the substrate with high planarity differences during die attach process. On the other hand, bond delay parameter refers to the amount of time the bond force is applied onto the die during the bonding of the die to substrate. In regards to the DAF voids, the bond delay is used to ensure a solid and equal bonding between the substrate and die by allowing the adhesive to flow and distribute evenly throughout the bond region. In general, the amount of time is often based on the adhesive properties and the size of the die being bonded.

DOE summary of the bond temperature and bond delay in response to DAF void and die crack are shown in the Table I. Die crack inspection was conducted at three process which is the die attach process, molding process and package singulation step. Based on the simulation data, the crack only occurs at molding process where the high packing pressure on the die create an "pivot" effect at the DAF void location which causes the crack initiated from the top of die. Post mold process up until the singulation step did not observe any additional die crack. The die crack units exhibit the same defect signature and location. Two factor two level DOE was employed to evaluate the key parameters in response to DAF void percentage. It is observed that the best parameter setting is Leg 4 which the bonding temperature is at 140ºC and bonding time at 500ms as shown in Fig. 10. By comparing Leg 1 and Leg 3, the average DAF void percentage decreased by about 9%. This shows that bond temperature has significant effect on DAF void reduction. While the bond delays are to encourage the heat absorption for the DAF to melts and adhere properly to the substrate. Based on the SAT results on the unit as shown in Table II, it is observed that the void region is significantly lower when the bonding temperature and bond time is at the higher side in comparison to the parameters at low side. This is because the additional heat promotes DAF to melt and filles the uneven planarity of the substrate and the increased in bond delay provide sufficient time for the DAF to absorb the heat supplied.

Table I DOE summary in response to DAF void

Leg	Bond Delay (ms)	Bond temp (°C)	Result			Total die crack (%)	Average Void (%)
			Post DA	Post Mold	Post Saw		
1	Low (300)	Low (100)	0/28	2/28	2/28	7.14	10.70
2	High (500)	Low (100)	0/28	1/28	1/28	3.57	4.15
3	Low (300)	High (140)	0/28	0/28	0/28	0	1.52
4	High (500)	High (140)	0/28	0/28	0/28	0	0.70

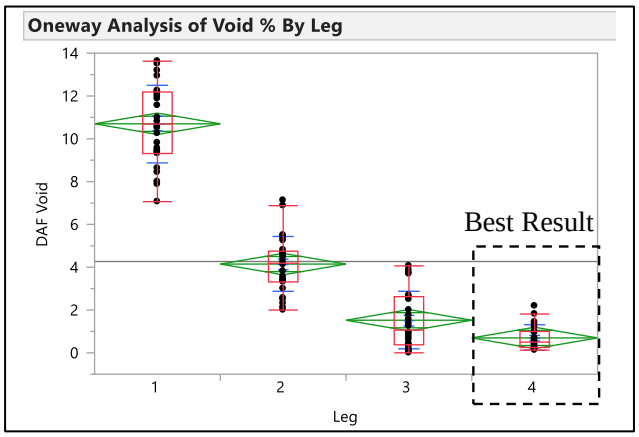
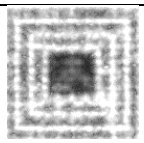
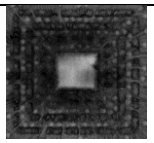
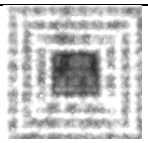
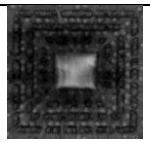
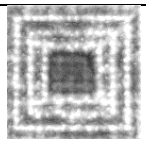
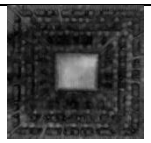
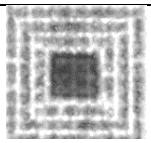
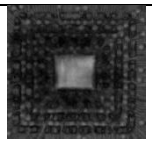


Fig. 10 DOE parameter settings in response to DAF void percentage.

Table II SAT results and observation

Leg	SAT Results		Observation
	Through Scan	C-Scan	
1			Plenty of voids Die crack
2			Voids localized on left and right Die crack
3			Small number of voids is still visible on right side No die crack
4			Minimum void is observed at the right side No die crack

IV. CONCLUSION

It is important to note that voids can also affect the thermal and electrical performance of the package, which can lead to further reliability issues. Therefore, it is crucial to minimize void formation during the die attach process to ensure the overall reliability and performance of the package. This study provides valuable insights into the correlation between substrate co-planarity, DAF void formation, and die crack in BGA packages. Generally, they have the characteristic of fixed location and similar pattern, which are correlative with substrate surface topography .By optimizing the die attach parameters and improving substrate design, the occurrence of DAF voids can be effectively reduced, leading to improved reliability and performance of the package.

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REFERENCES

[1] Zhang, Rongwei, and Vikas Gupta. "Void control in die attach joint." SOLID STATE TECHNOLOGY 61.4 (2018): 20-23.

[2] Bin Zhang, Ning Chen and Feizhou Zhang, "Methods for searching the cause of crack," Proceedings of the 12th International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2005. IPFA 2005., 2005, pp. 222-225, doi: 10.1109/IPFA.2005.1469166.

[3] Y. Su, D. Bai, V. Huang, W. Chen and T. S. Xian, "Effect of transfer pressure on die attach film void performance," 2009 11th Electronics Packaging Technology Conference, 2009, pp. 754-757, doi: 10.1109/EPTC.2009.5416448.

[4] N. Kao, Y. P. Wang, S. Chou, Y. L. Tsai and T. D. Her, "Substrate designs to improve die crack damage in CSP," Advances in Electronic Materials and Packaging 2001 (Cat. No.01EX506), Jeju, Korea (South), 2001, pp. 444-449, doi: 10.1109/EMAP.2001.984025.